REMARKS

Applicants note the filing of an Information Disclosure Statement herein on July 12, 2000 and note that no copy of the PTO-1449 was returned with the outstanding Office Action. Applicants respectfully request that the information cited on the PTO-1449 (which is the same as that of record to that date in the parent application hereto) be made of record herein.

The Office Action mailed September 11, 2001, has been received and reviewed. Claims 1 through 18 are currently pending in the application. Claims 1 and 2 have been withdrawn from consideration as being drawn to a non-elected invention. Claims 3 through 18 stand rejected. Applicants have added claims 19 through 22 and have amended claim 3, and respectfully request reconsideration of the application as amended herein.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,428,244 to Segawa et al.

Claims 3 through 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Segawa et al.(U.S. Patent No. 5,428,244). Applicants respectfully traverse this rejection, as hereinafter set forth.

Segawa et al. discloses a method of manufacturing a semiconductor device having a metallic silicide film wherein the adhesion properties between the metallic silicide film and an overlying dielectric layer are improved. The methods taught by Segawa et al. for forming improved adhesion qualities between a metallic silicide film and an overlying dielectric layer require that the overlying dielectric layer be deposited in a chemical vapor deposition chamber at a temperature of between 650 °C and 840 °C. Segawa et al. does not teach or suggest the deposition of a dielectric layer at a temperature lower than 650 °C.

Segawa et al. fails to establish a *prima facie* case of obviousness because all of the claim limitations of claims 3 through 18 are not taught or suggested by Segawa et al. Furthermore, one of ordinary skill in the art would not have modified Segawa et al. to make obvious the claims of

the present invention because there is no motivation in the art or in Segawa et al. to do so. M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, **there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings**. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

As acknowledged in the Official Action, Segawa et al. fails to specify the deposition of a dielectric cap layer at a sufficiently low temperature. *See, Official Action* at p. 2. Thus, Segawa et al. fails to meet the third requirement for establishing a *prima facie* case of obviousness because all of the claim limitations are, admittedly, not taught by Segawa et al. Further, Applicants disagree with the Examiner's assertion that a person having ordinary skill in the art would have found it obvious to modify Segawa et al. to arrive at the method of the present claims. Without Applicants' disclosure, there is absolutely no motivation to lower the deposition temperature of the dielectric cap of Segawa et al. to about 600 °C or less. Motivation is lacking because Segawa et al. does not realize, or disclose, the problems that the methods claimed in the present invention solve.

Independent claim 3 is amended herein to specifically recite "depositing a dielectric cap layer over said metallic silicide film at a temperature below about 600 °C." This amendment further clarifies at least one temperature range that is sufficiently low as originally claimed. Nowhere does Segawa et al. teach or suggest such a limitation. Instead, Segawa et al. specifically indicates that the required deposition temperature of a dielectric layer to form the structure of Segawa et al. is at least 650 °C and may be as high as 840 °C. Even in those Examples disclosed by Segawa et al. where the deposition temperature in a CVD reactor was below 600 °C for deposition of a metallic silicide film, the "chamber temperature is increased up

to 650 °C to 700 °C." Such temperature ranges for dielectric layer deposition do not teach the limitations claimed by the present invention. Therefore, claim 3 is allowable over Segawa et al. because all of the claim limitations are not taught by the cited prior art reference. *See, In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Segawa et al. also fails to make obvious independent claim 3 because there is no suggestion or motivation to a person of ordinary skill in the art to modify Segawa et al. to arrive at the method claimed by claim 3. Segawa et al. is directed towards the formation of a metallic silicide structure having a strong adhesion with a dielectric layer. The present invention, however, provides a method for eliminating pitting on a silicon substrate during gate stack etching. It has been found that the formation of silicon clusters in metallic silicide films may result in the undesired pitting of a silicon substrate. The formation of silicon clusters in a metallic silicide film has been specifically found to occur when the step of forming a dielectric cap over a metallic silicide film exceeds 600 °C. *See, Specification* at p. 5, lines 11-24. Segawa et al. does not recognize this fact, and indeed, does not even recognize the pitting problems that are solved by the method claimed by claim 3. A person attempting to reduce the pitting of a silicon structure, armed only with the disclosure of Segawa et al. and the knowledge of one having ordinary skill in the art, would not find it obvious to lower the dielectric layer deposition temperature of Segawa et al. Further, one of ordinary skill in the art would not lower the dielectric layer deposition temperature to below 650 °C to form the structure of Segawa et al. because Segawa et al. expressly discloses that such a deposition temperature must be greater than 650 °C. Indeed, Segawa et al. seems to indicate that deposition of a dielectric layer at a temperature below 650 °C is not possible because Segawa et al. teaches that the deposition temperature for the dielectric layer must be raised to at least 650 °C, even when the deposition chamber is already at 600 °C.

Without the disclosure of the present invention, that the deposition temperature for a dielectric layer is preferably below about 600 °C to reduce the formation of silicon clusters that cause silicon substrate pitting in a metallic silicide, one having ordinary skill in the art would not

find it obvious to lower the dielectric layer deposition temperature of Segawa et al. below about 600 °C. Furthermore, the fact that Segawa et al. teaches that the dielectric deposition temperature must be above 650 °C precludes a *prima facie* obviousness rejection of claim 3 because there is no motivation to reduce the deposition temperature of Segawa et al. to a temperature within the temperature range included as a limitation in claim 3.

Claims 4 through 16 depend from independent claim 3 and are therefore nonobvious because the independent claim from which they depend is nonobvious. *See, In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988) (dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious).

Furthermore, dependent claims 4 through 7 are independently allowable because Segawa et al. fails to teach or suggest the claim limitations of those claims. Specifically, Segawa et al. does not disclose a dielectric layer deposition temperature of between 400 °C and 600 °C as recited in claim 4. Similarly, a dielectric layer deposition temperature of about 500 °C, as claimed by claim 5, is not taught. The limitation recited by claim 6 is admittedly nonobvious by the statements made in the Official Action. *See, Official Action* at p. 3. Likewise, Segawa et al. does not teach the limitation of forming a dielectric cap layer "at a temperature sufficiently low to preclude formation of silicon clusters in said metallic silicide film" as recited by claim 7.

Independent claim 17 is also rejected under 35 U.S.C. § 103(a) over Segawa et al. in light of Chang et al. (United States Patent 5,438,006). However, independent claim 17 is allowable over the rejection because a *prima facie* case of obviousness cannot be established by the cited references.

Independent claim 17 specifically recites the limitation of "forming a dielectric cap on said metallic silicide film at a sufficiently low temperature that said metallic silicide film remains in said non-annealed state" (emphasis added). The Official Action acknowledges the fact that Segawa et al. fails to teach deposition at such a temperature. *See, Official Action* at p. 3. Chang et al. also fails to teach or suggest the deposition of a dielectric layer at such a temperature. Thus, neither reference, either alone or in combination, satisfies the *prima facie* obviousness

requirement that the references teach all of the claim limitations. *See, In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Additionally, there is no motivation for one of skill in the art to reduce the dielectric layer deposition temperatures of Segawa et al. to a "sufficiently low temperature" that would make obvious claim 17. Change et al. provides no such motivation, and in fact fails to even discuss deposition temperatures. Furthermore, one of skill in the art would not be motivated to use the method of claim 17 without access to the disclosure of the present invention. Just as Segawa et al. fails to make obvious claim 3, Segawa et al. fail to make obvious claim 17.

Claim 18 depends from claim 17, an allowable independent claim, and is therefore also allowable. *See, In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). Furthermore, claim 18 recites the formation of a dielectric cap "at a temperature below about 600 °C," which is not taught by either Segawa et al. or Chang et al. Thus, a *prima facie* case of obviousness with respect to claim 18 is lacking. *See, In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Additional claims 19 through 22 are not obvious in light of the cited references because claim 19 includes the limitations of claim 3 and claims 20 through 22 are dependent on allowable independent claim 19.

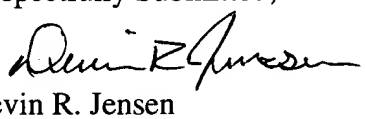
ENTRY OF AMENDMENTS

The amendments to claim 3 above, and the addition of claims 19 through 22, should be entered by the Examiner because the amendments and additions are supported by the as-filed specification and drawings and do not add any new matter to the application.

CONCLUSION

Claims 3 through 22 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully Submitted,



Devin R. Jensen
Registration Number 44,805
Attorney for Applicants
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110
Telephone: (801) 532-1922

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Enclosure: Version With Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

3. (Amended) A method of forming a gate stack, comprising:
forming a gate dielectric layer on a silicon substrate;
forming a polysilicon layer on top of the gate dielectric layer;
subjecting said polysilicon layer to an ion implantation of impurities;
depositing a metallic silicide film in a non-annealed state atop said polysilicon layer; and
depositing a dielectric cap layer over said metallic silicide film at a [sufficiently low] temperature below about 600 °C. [such that the metallic silicide film remains in said non-annealed state.]

19. A method of forming a gate stack, consisting essentially of:
forming a gate dielectric layer on a silicon substrate;
forming a polysilicon layer on top of the gate dielectric layer;
subjecting said polysilicon layer to an ion implantation of impurities;
depositing a metallic silicide film in a non-annealed state atop said polysilicon layer; and
depositing a dielectric cap layer over said metallic silicide film at a temperature below about 600 °C such that the metallic silicide film remains in said non-annealed state.

20. The method of claim 19, wherein said depositing a dielectric cap layer over said metallic silicide film is effected at a temperature of between 400°C and 600°C.

21. The method of claim 19, wherein said depositing a dielectric cap layer over said metallic silicide film is effected at a temperature of about 500°C.

22. The method of claim 19, wherein said depositing a dielectric cap layer over said metallic silicide film is effected at a temperature sufficiently low to preclude formation of silicon clusters in said metallic silicide film.